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(71) Applicant: **Yozan Inc.**
Tokyo 155-0031 (JP)

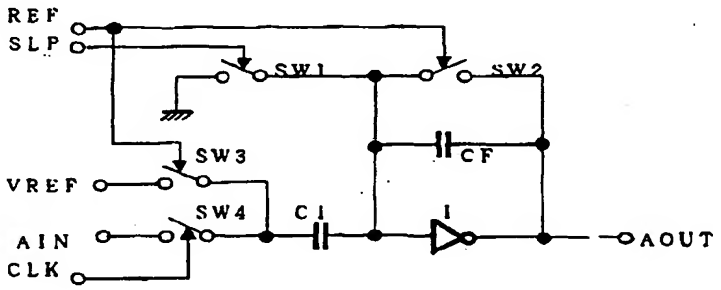
(72) Inventors:
- **Zhou, Changming**
  Tokyo 155-0031 (JP)
- **Shou, Guoliang**
  Tokyo 155-0031 (JP)
- **Lin, Shengmin**
  Tokyo 155-0031 (JP)
- **Tomatsu, Takashi**
  Tokyo 155-0031 (JP)
- **Chen, Jie**
  Tokyo 155-0031 (JP)

(74) Representative:
Grünecker, Kinkeldey,
Stockmair & Schwanhäusser
Anwaltssozietät
Maximilianstrasse 58
80538 München (DE)

(54) Inverting amplifying circuit

(57) An inverting amplifying circuit for outputting an inversion of an input with good linearity, having an inverter circuit, a feedback capacitance, an input capacitance, a first refresh switch, a second refresh switch and a sleep switch. A sleep voltage is input through the sleep switch to the inverter circuit for minimizing the electrical power consumption.

Fig. 1



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Description

Detailed Description of the Present Invention

Background of the Invention

Field of the Invention

The present invention relates to an inverting amplifying circuit, particularly to an inverting amplifying circuit having odd number of CMOS inverters serially connected from the first to the last stages. An output of the last stage CMOS inverter is fed through a feed back capacitance back to an input of the first stage. An input voltage is input through an input capacitance to the input of the first stage CMOS.

Prior Art

The inverting amplifying circuit of this type is advantageous for transferring the input voltage with drive-ability, high accuracy and good linearity to the output when analog voltage calculation is performed. The inventors of the present invention have proposed a matched filter for mobile cellular communication having a lot of portions such as a sampling and holding circuit, a multiplication circuit and an addition circuit, to which the inverting amplifying circuit is applied.

Fig. 23 shows a conventional inverting amplifying circuit. A feedback capacitance CF is connected between input and output of inverting circuit I consisting of odd number of CMOS inverters serially connected. The output of the inverting circuit I is connected through a switch SW7 to the capacitance CF, and the input is connected to an input capacitance CI. An analog input voltage AIN is connected to CI through a switch SW4 which is controlled by a clock CLK. A switch SW8 is connected through a switch SW3 between SW4 and CI so that CF is short-circuited by SW2. The switch SW8 connects a refresh voltage VREF or the ground voltage to SW3. VREF is selected when refreshed, and the ground voltage is selected when sleep mode for preventing electrical power consumption. When refreshed, both of SW2 and SW3 are closed and SW8 selects VREF so that VREF is impressed to an input of CI as well as CF is short-circuited. VREF is equal to a threshold voltage Vd/2 (Vd: a supply voltage of the inverter) of the inverter circuit, so Vd/2 is generated at the input of the inverter circuit I when CF is short-circuited. The voltages of input and output are equal to each other of not only CF but also of CI. A residual charge is cancelled. An offset voltage due to the residual charge is deleted and a calculation is accurate. The input of the inverter circuit is connected through SW1 to SW8. When sleep mode, SW1 is closed, SW7 is connected to SW8 and SW8 is connected to the ground, then the input of the inverter is connected to the ground. SW2 is opened. The electrical power consumption of the inverter is stopped.

The inverting amplifying circuit above is accurate in calculation and of low electrical power consumption. However, lower power consumption as well as smaller circuit size are required.

Fig.24 shows an inverting amplifying circuit proposed in the patent publication before examination Hei07-094957. In the circuit, similar portions to those in Fig.23 are designated by the same references, and descriptions therefor are omitted. The inverter circuit I consists of three CMOS inverters I51 to I53 serially connected. A serial circuit of a resistance R and a capacitance Cm is connected between the first and second stages I51 and I52 for preventing unexpected and unstable oscillation by its phase compensation function. There is a problem that an output voltage AOUT has an offset voltage occurs when thresholds of nMOS and pMOS of each CMOS are different due to production errors.

Summary of the Invention

The present invention, is invented so as to solve the conventional problem and has an object to provide an inverting amplifying circuit of lower power consumption and high accuracy.

An inverting amplifying circuit according to the present invention has a sleep switch for connecting an input of a inverting circuit to the ground voltage.

Brief Description of Drawings

Fig.1 is a circuit diagram of the first embodiment according to the present invention.
Fig.2 is a circuit diagram of the second embodiment.
Fig.3 is a circuit diagram of the third embodiment.
Fig.4 is a circuit diagram of the fourth embodiment.
Fig.5 is a circuit diagram of an inverter circuit in the embodiments above.
Fig.6 shows another inverter circuit.
Fig.7 shows the fifth embodiment.

Fig.8 is a circuit diagram of a switch in Fig.7.
Fig.9 is a circuit diagram of a variation of the switch in Fig.8.
Fig.10 shows further another switch.
Fig.11 shows a variation of the switch in Fig.10.
Fig.12 is a circuit diagram of the sixth embodiment.
Fig.13 shows the seventh embodiment.
Fig.14 shows the eighth embodiment.
Fig.15 shows the ninth embodiment.
Fig.16 shows the tenth embodiment.
Fig.17 shows a gate circuit for providing a sleep signal.
Fig.18 shows a variation of the circuit in Fig.17.
Fig.19 shows the eleventh embodiment.
Fig.20 shows the twelfth embodiment.
Fig.21 shows the thirteenth embodiment.
Fig.22 shows the fourteenth embodiment.
Fig.23 shows a conventional inverting amplifying circuit.
Fig.24 shows another conventional circuit.

Preferred Embodiment of the Present Invention

Fig.1 shows the first embodiment of an inverting amplifying circuit. There is provided an inverter circuit I having odd number of CMOS inverters, typically three CMOS inverters. An output of the circuit I is connected through a feedback capacitance CF to an input thereof. An input capacitance CI is connected to the input of I, and an input voltage AIN is connected through a switch SW4 to CI. The switch SW4 is controlled by a clock CLK.

A refresh switch SW2 is connected to opposite terminals of CF so that an electrical charge of CF is cancelled because CF is short-circuited. Then, the input and output of the inverter circuit I is short-circuited when SW2 is closed, so a threshold voltage of the inverter circuit occurs at the input and output of I. A refresh voltage VREF is connected through a refresh switch SW3 to an input of CI. The input and output of CI are impressed by the same voltage. An electrical charge is cancelled in CI. The threshold voltage is designed to be Vd/2, a half of a supply voltage Vd. The refresh switch is controlled by a refresh signal REF.

In addition, the switch SW1 is opened when the circuit is in refesh mode

A sleep switch SW1 connected to the ground is connected to an input of the inverter circuit. The ground voltage is connected through SW1 to the input of I when SW1 is closed. The inverter circuit becomes a saturation area so that a current through CMOSs are prevented. An electrical power consumption is stopped. The switch SW1 is controlled by a sleep signal SLP.

In addition, the switch SW2 is opened when the circuit is in sleep mode.

The circuit is simplified by omitting the switch SW7 in the conventional circuit. The circuit size and the production cost are decreased and the yielding is improved. The sleep switch can be the supply voltage Vd instead of the ground.

Fig.2 shows the second embodiment, in which similar portions to those in Fig.1 are designated by the same references and the descriptions therefor are omitted. A switch SW5 is provided between the outputs of the inverter circuit I and the feedback capacitance in addition to the circuit of Fig.1. The switch SW5 is opened when sleep mode so that the output of the inverter circuit I is disconnected from the output for outputting the analog output voltage AOUT of the inverting amplifying circuit. For this inverted control logic, the sleep signal is supplied through an inverter IC. The output of I is Vd when sleep mode. This voltage is not transferred to the circuits following to the inverting amplifying circuit so that the circuits are not influenced by the voltage Vd. The supply voltage may be connected to the sleep switch instead of the ground voltage.

Fig.3 shows the third embodiment, in which similar portions to those in Fig.1 are designated by the same references and the descriptions therefor are omitted. A switch SW6 is provided between the input of the inverter circuit I and the output of the input capacitance instead of the sleep switch of Fig.1. The switch SW6 connects the input of the inverter circuit to the output of CI or the ground. The ground is selected when sleep so that the input of the inverter circuit I is disconnected from circuits in advance to the inverting amplifying circuit. The ground voltage connected to the inverter circuit is not transferred to the circuits so that the circuits are not influenced by the ground voltage. The input of the capacitance CF is connected to between CI and SW6 in Fig.3, however, it may be connected between SW6 and the inverter circuit. Since the capacitances CI and CF are directly connected in Fig.3, it is advantageous that these capacitances can be adjacently arranged in an integrated circuit.

Fig.4 shows the fourth embodiment, in which similar portions to those in Fig.1 are designated by the same references and the descriptions therefor are omitted. Both of the switches SW5 and SW6 are used for preventing the influences to the circuits in advance and following to the inverting amplifying circuit.

Fig.5 exemplarily shows the inverter circuit I used in the above embodiments. The inverter circuit I has three CMOS inverters INV1, INV2 and INV3 serially connected. A phase compensation circuit is connected to the second inverter INV2 consisting of a capacitance CC and a MOS resistance MR serially connected. The phase compensation circuit increases a phase margin of the feedback system consisting of the inverter circuit I and the feedback capacitance CF. A grounded capacitance is connected to an output of the third stage inverter INV3 for preventing unexpected and unstable oscillation by reducing high frequency component.

Fig.6 shows another inverter circuit. A CMOS resistance CMR is connected between the first stage INV1 and the second stage INV2. A phase compensation circuit is connected between the input and output of the third stage inverter INV3. The phase compensation circuit consists of a capacitance CC and a resistance R serially connected. The phase compensation circuit increases a phase margin of the feedback system consisting of the inverter circuit I and the feedback capacitance CF.

Fig.7 shows the fifth embodiment, in which similar portions to those in Fig.1 are designated by the same references and the descriptions therefor are omitted. A switch SW71 of three inputs and one output is connected to the input of the input capacitance, and a switch SW72 of two inputs and one output is connected between the first and second inverters INV1 and INV2. Similar to the circuit in Fig. 5, a phase compensation circuit is connected between the input and output of the inverter INV2.

The switch SW2 is closed both in the refresh mode and the sleep mode.

As shown in Fig.8, the switch SW71 is controlled by the signal REF and SLP so that its input is connected to the ground when SLP is valid, to Vref when REF is valid and otherwise to AIN.

The switch SW71 con be omitted because the input of the inverter circuit I becomes the ground voltage when SW2 is closed.

As shown in Fig.10, the switch SW72 is controlled by SLP so that the input is connected to the ground when SLP is valid and otherwise to the output (shown by Vi4) of INV1. SW71 is also connected to the ground when SLP is valid. The CMOS inverters INV1 to INV3 become the saturation area so that the electrical power consumption is stopped.

Fig.9 shows a variation of the switch SW71. Instead of the ground, the supply voltage Vd is connected to the input of SW71. A similar effect is obtained. Fig.11 shows a variation of the switch SW72 which is connected at its input to the supply voltage Vd instead of the ground. The switches SW71 and SW72 have corresponding polarities. The circuits of Fig.8 and Fig.10 correspond to each other, and Fig.9 and Fig.11 correspond to each other.

Fig.12 shows the sixth embodiment, in which similar portions to those in Fig.7 are designated by the same references and the descriptions therefor are omitted. The switch SW72 of two inputs and one output is connected between the second and third inverters INV2 and INV3. A similar effect is obtained. As for polarities of the switches, SW72 is connected to Vd when SW71 is connected to the ground, and SW72 is connected to the ground when SW71 is connected to Vd. The switch SW2 is closed both in the refresh mode and the sleep mode.

Fig.13 shows the seventh embodiment, in which similar portions to those in Fig.7 are designated by the same references and the descriptions therefor are omitted. The switch SW72 is connected to the output of the third inverter INV3. A similar effect is obtained. As for polarities of the switches, SW72 is connected to the pound when SW71 is connected to the ground, and SW72 is connected to Vd when SW71 is connected to Vd.

Fig.14 shows the seventh embodiment, in which similar portions to those in Fig.7 are designated by the same references and the descriptions therefor are omitted. The switch SW72 is connected to the input of the inverter INV1. A similar effect is obtained. As for polarities of the switches, SW72 is connected to Vd when SW71 is connected to the ground, and SW72 is connected to the ground when SW71 is connected to Vd.

Fig.15 shows the eighth embodiment, in which similar portions to those in Fig.7 are designated by the same references and the descriptions therefor are omitted. Instead of INV1, a NOR gate G9 is connected between CI and INV2. The gate G9 receives the output of CI and SLP so as to invert the output of CI when SLP is invalid, that is, not sleep mode. The gate G9 outputs "0" when SLP is valid so as to connect the input of INV2 to the ground. The gate inverts small voltage change of the output of CI substantially equal to Vd/2. Any gate circuits equivalent to the gate G9 can be applied, and one or both of the second and third inverters INV2 and INV3 can be substituted by the gate circuits. The output of the date G9 should have polarity corresponding to the circuits Fig.8 and 9, similarly to the above. When INV1 or INV3 is substituted by G9, the switch SW71 of Fig.8 is used, and when INV2 is substituted by G9, the switch of Fig.9 is used. The switch for sleep mode is omitted by using the gate circuit, so the circuit size becomes smaller.

Fig.16 shows the ninth embodiment, in which similar portions to those in Fig.7 are designated by the same references and the descriptions therefor are omitted. Instead of INV1, a NAND gate G10 is connected between CI and INV2. The gate G9 receives the output of CI and SLP so as to invert the output of CI when SLP is invalid, that is, not sleep mode. The gate G9 outputs "1" when SLP is valid so as to connect the input of INV2 to Vd. The gate inverts small voltage change of the output of CI substantially equal to Vd/2. Any gate circuits equivalent to the gate G10 can be applied, and one or both of the second and third inverters INV2 and INV3 can be substituted by the gate circuits. The output of the date G9 should have polarity corresponding to the circuits Fig.8 and 9, similarly to the above. The switch for sleep mode is omitted by using the gate circuit, so the circuit size becomes smaller.

Fig.17 shows a circuit for generating a control signal of sleep mode. The circuit has an AND gate G11 for receiving SLP and an inversion of REF. When REF is invalid, an signal SLP' equal to SLP is output, and when REF valid, SLP' is always "0". It means that the sleep signal SLP' is superior to the refresh signal. The sleep operation is executed without fail if the sleep signal is independently generated from REF.

Fig.18 shows another circuit for SLP'. There is provided a OR gate G12 for receiving SLP and REF. If both of the CI and CMOS inverters are connected to the ground when both in the refresh and sleep mode, this circuit is advantageous.

Fig. 19 shows the tenth embodiment, in which similar portions to those in Fig.7 are designated by the same references and the descriptions therefor are omitted. The CMOS inverters INV1 to INV3 consist of pMOS and nMOS transistors P11 and N11, P12 and N12 and P13 and N13, respectively. The output of CI is connected only to the gate of nMOS N11 without connected to the pMOS P11. The output of INV1 is connected only to the gate of nMOS N12 without connected to the pMOS P12, and the output of INV2 is connected only to the gate of nMOS N13 without connected to the pMOS P13. The pMOSs P11 to P13 are connected at their gate to a common bias voltage VB.

When VB is constant, P11 to P13 are of a function of a constant current source having a constant current between the source and drain. The current changes as VB changes. The voltage drop in nMOSs can be changed so as to decreased the offset voltage.

Table 1 shows a relationship between the threshold voltages of nMOS and pMOS and the offset voltage of the circuit of Fig.24 and a relationship beween the offset voltage and the bias voltage.

Table 1

Offset Voltage and Bias Voltage			
Circuit of Fig.24		Circuit of Fig.9	
Threshold Voltage	Offset Voltage	Bias Voltage	Offset Voltage
pMOS and nMOS have typical thresholds	-2.5mV	1.520 V	-0.10mV
pMOS has low threshold and nMOS has high threshold	363.0mV	2.176 V	0.50mV
pMOS has high threshold and nMOS has low threshold	-361.0mV	0.478 V	0.02mV

As will be understood from Table 1, the typical threshold of -2.5mV is decreased y the bias voltage to -0.10mV. The offset voltage of 363mV is decreased to 0.50mV when the threshold of nMOS is high, and -361mV to 0.02mV when the threshold of pMOS is high. The offset voltage is substantially cancelled by the bias voltage. The bias voltages for the conditions in Table 1 are 1.520V, 2.176V and 0.478V from the top to the bottom.

A function of MOS resistance for the phase compensation circuit can be obtained by the pMOS changeable in the current from the source to the drain. It means the phase compensation circuit can be smaller or omitted.

Fig.20 shows the eleventh embodiment, in which similar portions to those in Fig.19 are designated by the same references and the descriptions therefor are omitted. The relationship between the pMOSs and nMOSs are inverted. The analog input voltage AIN is input to the gate of pMOS P21, the output of P21 is input to the gate of P22, and the output of P22 is input to P23. VB is commonly input to the gate of N21, N22 and N23.

When VB is constant, N21 to N23 are of a function of a constant current source having a constant current between the drain and source. The current changes as VB changed. The voltage drop in pMOSs can be changed so as to decreased the offset voltage.

Fig.21 shows the twelfth embodiment, in which similar portions to those in Fig.19 are designated by the same references and the descriptions therefor are omitted. The first and second CMOS inveriers INV1 and INV2 are similar to those in Fig.19. The third CMOS inverter INV3 is similar to that in Fig.24. The dynamic range of the last stage inverter is increased in this embodiment wider than the circuits of Figs.19 and 20.

Fig.22 shows the thirteenth embodiment, in which similar portions to those in Fig.19 are designated by the came references and the descriptions therefor are omitted. A switch SWB is provided in addition to the circuit of Fig.19. The switch SWB receives VB and Vd for alternatively inputting VB or Vd to the gate of pMOSs p41 to p43. When Vd is connected, pMOSs are not conductive and the electrical power is cut off.

It is also possible nMOSs are used instead of pMOSs as the constant current source in the circuit of Fig.22.

Claims

1. An inverting amplifying circuit comprising:

an inverter circuit having an input and an output, said inverter circuit comprising odd number of CMOS inverters serially connected;
a feedback capacitance connected having an input and an output, said feedback capacitance being connected between said input and output of said inverter circuit;
an input capacitance having an input and an output, said input capacitance being connected at its output to said input of said inverter circuit for inputting an input voltage to said inverter circuit;
a first refresh switch connected between said input and output of said feedback capacitance for short-circuiting said feedback capacitance when refresh mode;
a second refresh switch connected to said input capacitance for inputting a refresh voltage equal to a threshold voltage of said inverter circuit to said input of said inverter circuit when refresh mode; and
a first sleep switch for connecting a first sleep voltage to a terminal of one of said CMOS inverters of said inverter circuit when sleep mode.

2. An inverting amplifying circuit as claimed in Claim 1, wherein said first sleep switch is connected to an input of said CMOS inverters of a first stage CMOS INVERTER, that is, said first sleep switch is connected to said input of said inverter circuit.

3. An inverting amplifying circuit as claimed in Claim 1, wherein said first sleep voltage is a ground voltage.

4. An inverting amplifying circuit as claimed in Claim 1, wherein said first sleep voltage is a supply voltage.

5. An inverting amplifying circuit as claimed in Claim 1, further comprising a first cut-off switch connected between said outputs of said inverter circuit and of said feedback capacitance, said cut-off switch being opened when sleep mode.

6. An inverting amplifying circuit as claimed in Claim 1, further comprising a second cut-off switch for selectively connecting said input of said inverter circuit to a saturation voltage when sleep mode or otherwise to said output of said input capacitance.

7. An inverting amplifying circuit as claimed in Claim 1, wherein said saturation voltage is a ground voltage.

8. An inverting amplifying circuit as claimed in Claim 1, wherein said saturation voltage is a supply voltage.

9. An inverting amplifying circuit as claimed in Claim 1, further comprising a second sleep switch connected to said input of said input capacitance for connecting a second sleep voltage to said input capacitance when sleep mode, said first and second sleep voltages corresponding to a polarity relationship between said terminal of said CMOS inverter and said input of said input capacitance.

10. An inverting amplifying circuit as claimed in Claim 9, wherein said first sleep switch is connected to an output said CMOS inverter of a last stage CMOS inverter, that is, said first sleep switch is connected to said output of said inverter circuit.

11. An inverting amplifying circuit as claimed in Claim 10, wherein said first and second sleep voltages are a ground voltage.

12. An inverting amplifying circuit as claimed in Claim 10, wherein said first and second sleep voltages are a supply voltage.

13. An inverting amplifying circuit as claimed in Claim 10, wherein one or more of said CMOS inverters are substituted by logic gates.

14. An inverting amplifying circuit as claimed in Claim 1, wherein said sleep switch is controlled by a sleep signal passing through a gate circuit which invalidate said sleep signal when refresh mode.

15. An inverting amplifying circuit as claimed in Claim 1, wherein each said CMOS inverters are substituted by a serial circuit of pMOS transistor and nMOS transistor, one of said transistor of the same polarity of each serial circuit being connected at its gate to said input capacitance, other transistor of each serial circuit being connected at its gate to a variable bias voltage.

16. An inverting amplifying circuit as claimed in Claim 1, wherein other said CMOS inverters than said CMOS inverter of a last stage are substituted by a serial circuit of pMOS transistor and nMOS transistor, one of said transistor of the same polarity of each serial circuit being connected at its gate to said input capacitance, other transistor of each serial circuit being connected at its gate to a variable bias voltage, said CMOS inverter of said last stage being connected at its gate to a conjuncture of said nMOS and pMOS transistors.

17. An inverting amplifying circuit as claimed in Claims 16, wherein said bias voltage can be a saturation voltage for cutting said transistor off to which said bias voltage is connected.

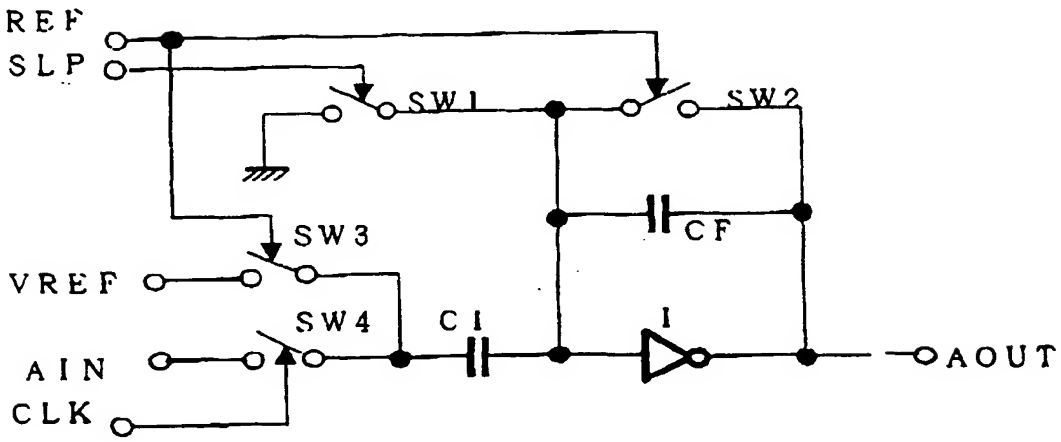
18. An inverting amplifying circuit as claimed in Claims 1 and 16, further comprising an oscillation prevention circuit for preventing unexpected or unstable oscillation of the feedback system consisting of said inverter circuit and said feedback capacitance.

19. An inverting amplifying circuit as claimed in Claim 18, said oscillation prevention circuit comprising a resistance and a capacitance serially connected, said oscillation prevention circuit being connected between said gate and a source of said transistor to which said input capacitance is connected.

20. An inverting amplifying circuit as claimed in Claim 19, said resistance is a MOS resistance.

21. An inverting amplifying circuit as claimed in Claim 18, said oscillation prevention circuit being connected between said transistor to which said input capacitance is connected one or more of other CMOS inverters or transistors than the last stage.

Fig.1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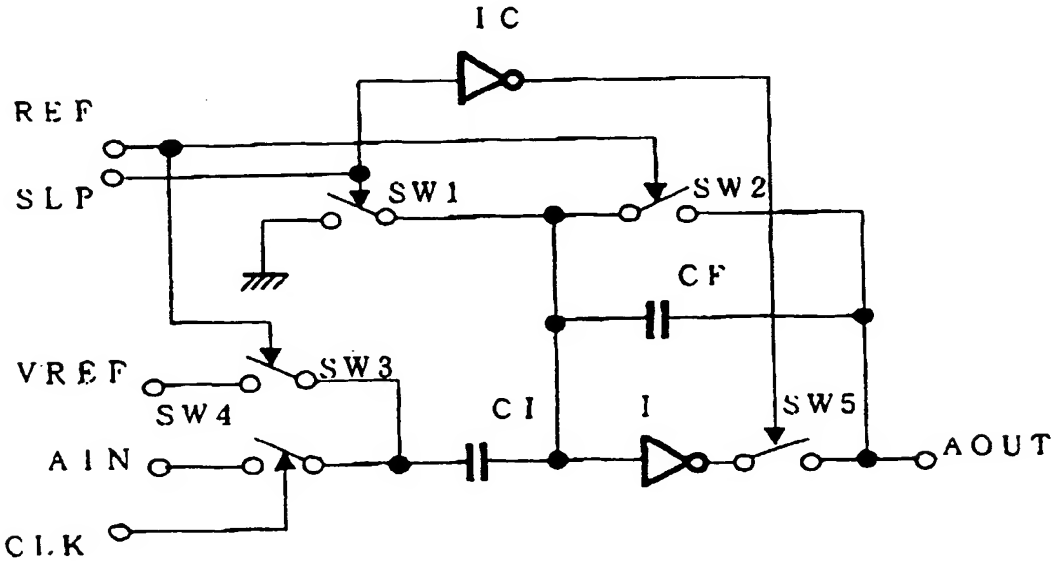
SW1
SW2
CF
SW3
VREF
SW4
CI
I
AIN
AOUT
CLK

Fig.2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REF
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Fig.3

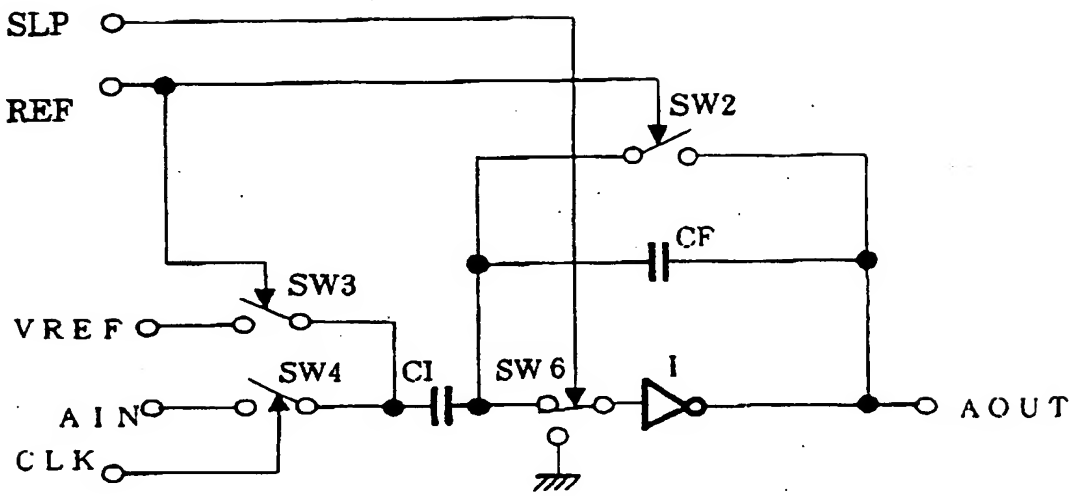


Fig.4

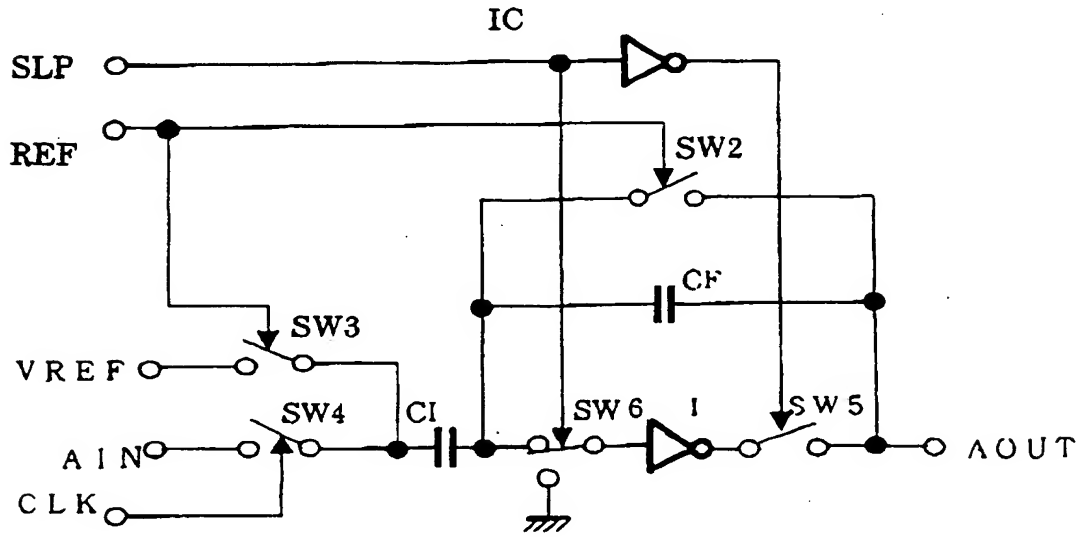


Fig.5

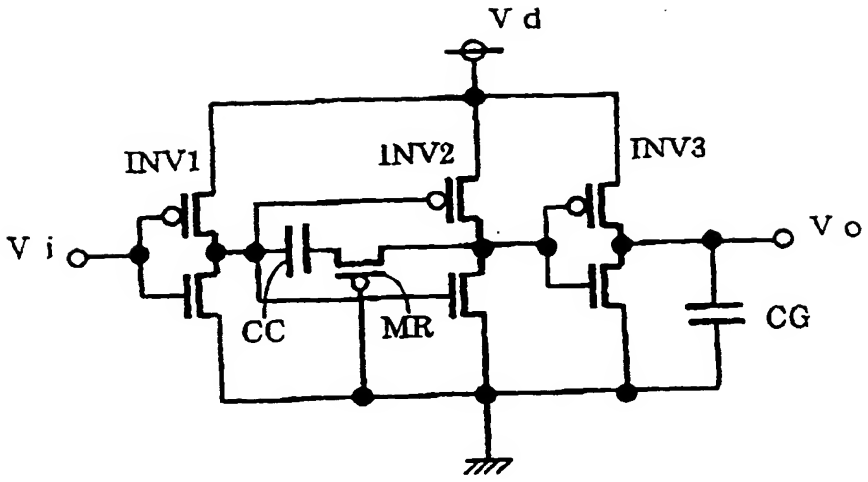


Fig.6

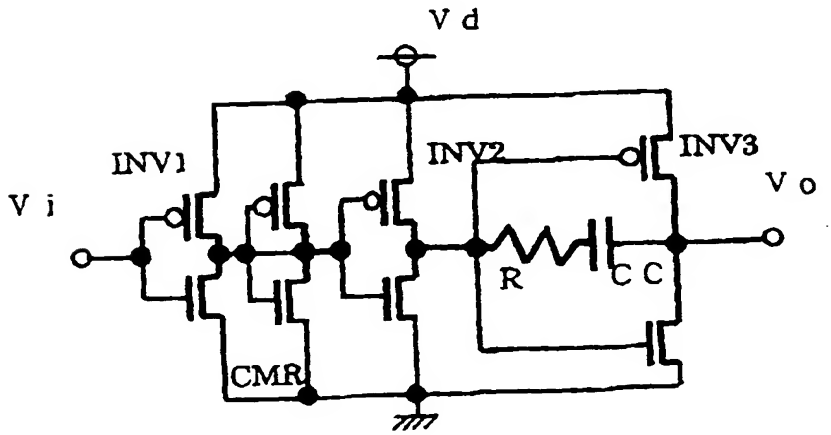


Fig. 7

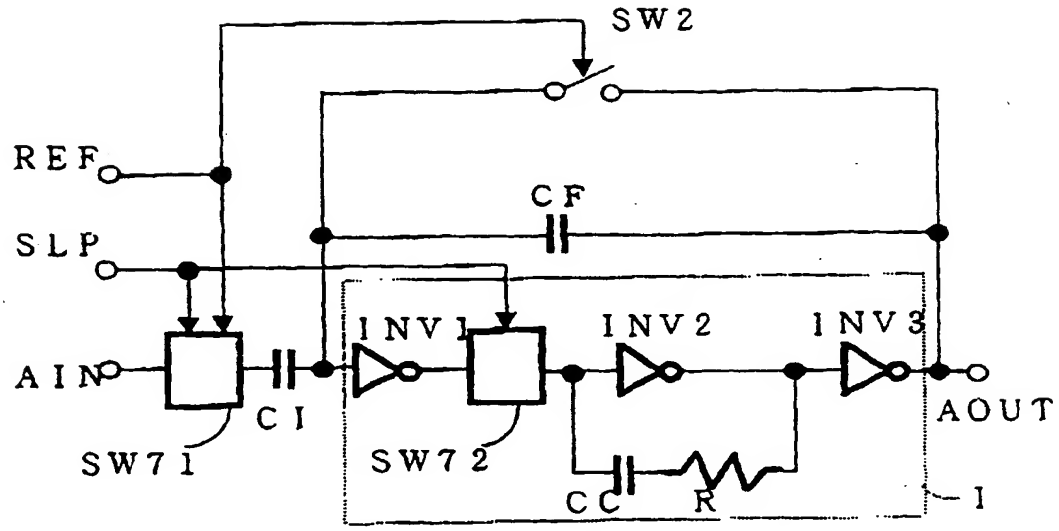


Fig. 8

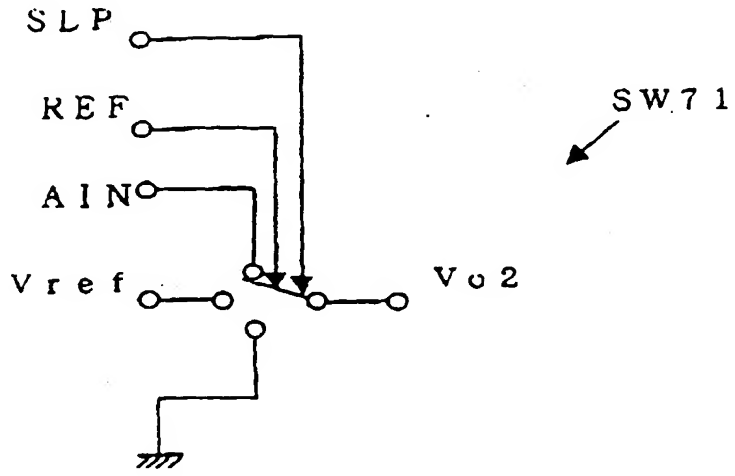


Fig.9

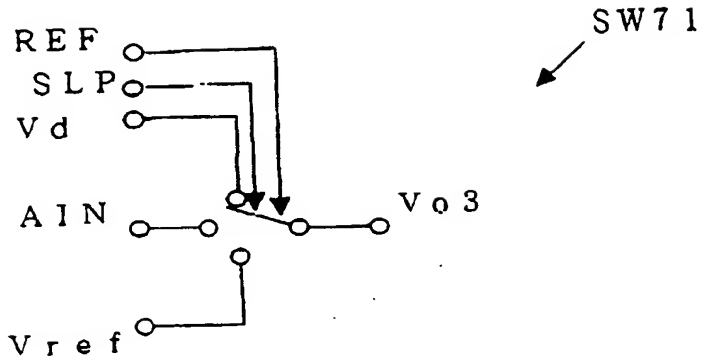


Fig.10

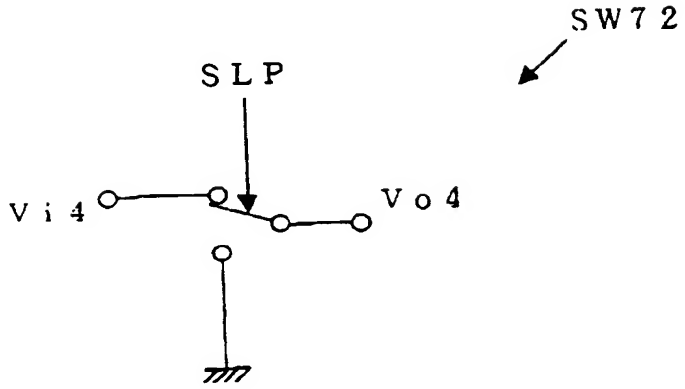


Fig.11

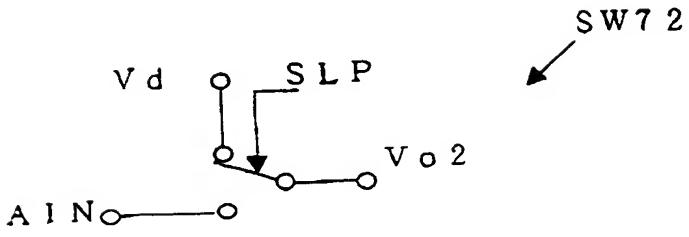


Fig.12

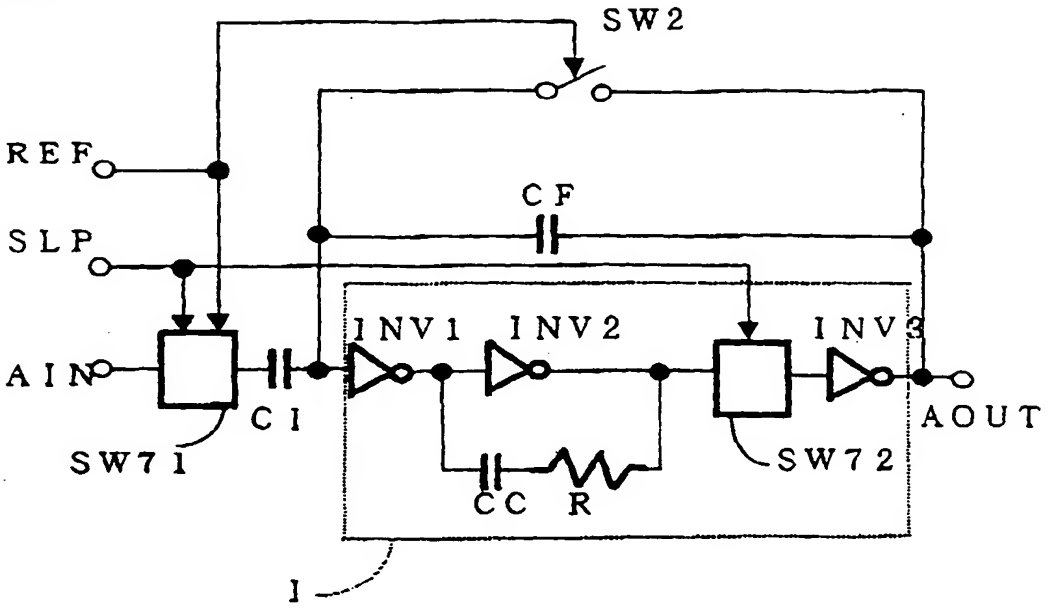


Fig.13

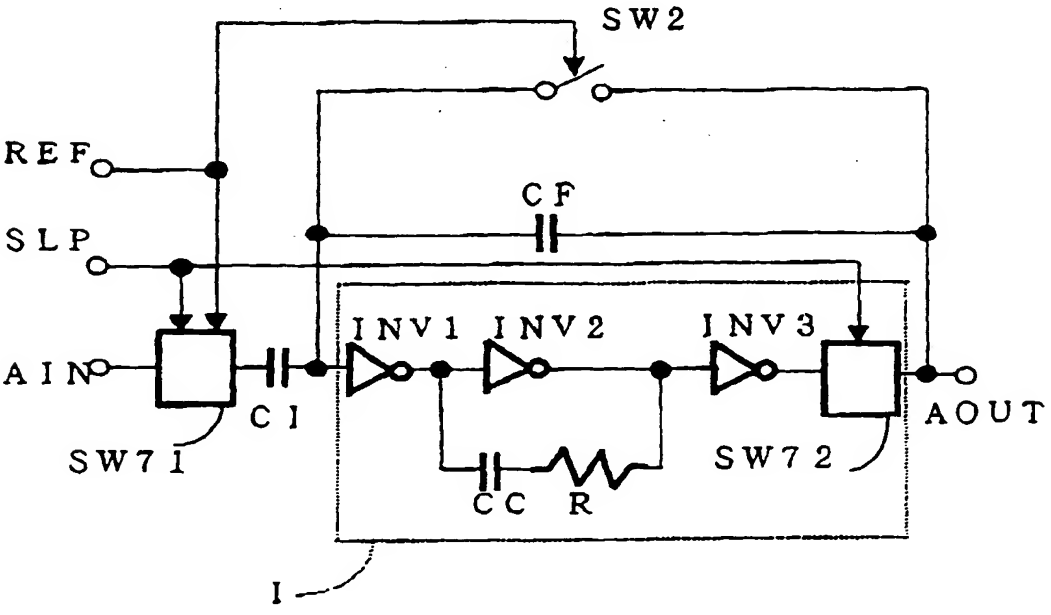
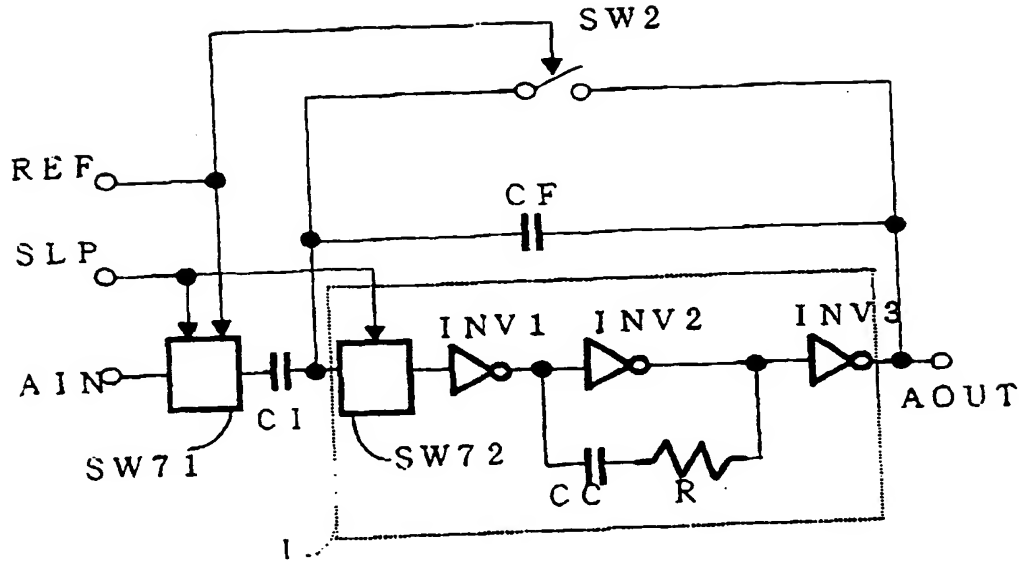


Fig.14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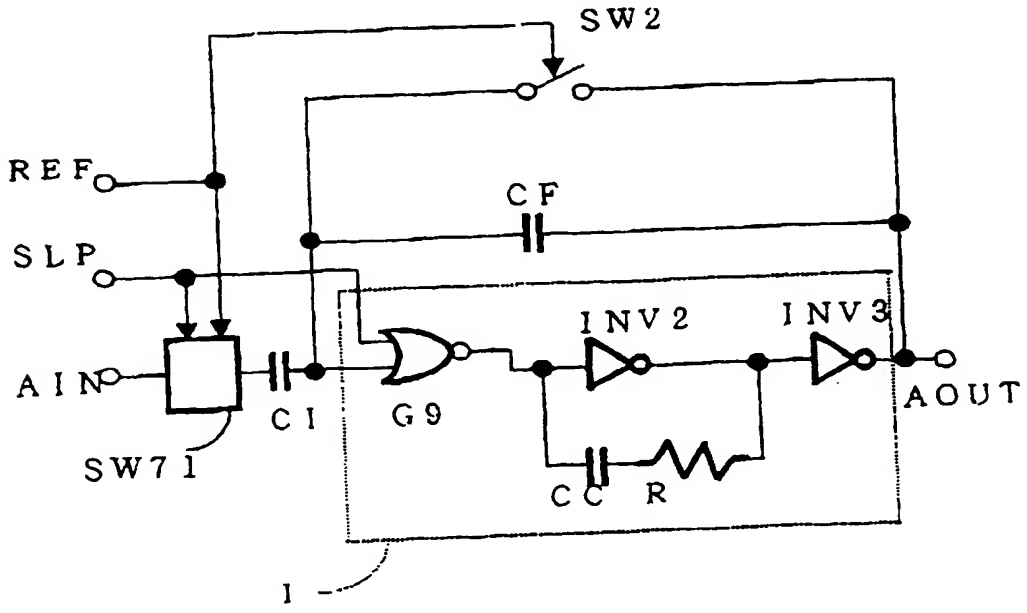
REF
CF
SLP
INV1
INV2
INV3
AIN
AOUT
CI
SW71
SW72
CC
R
I

Fig.15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SW71
CC
R
I

Fig.16

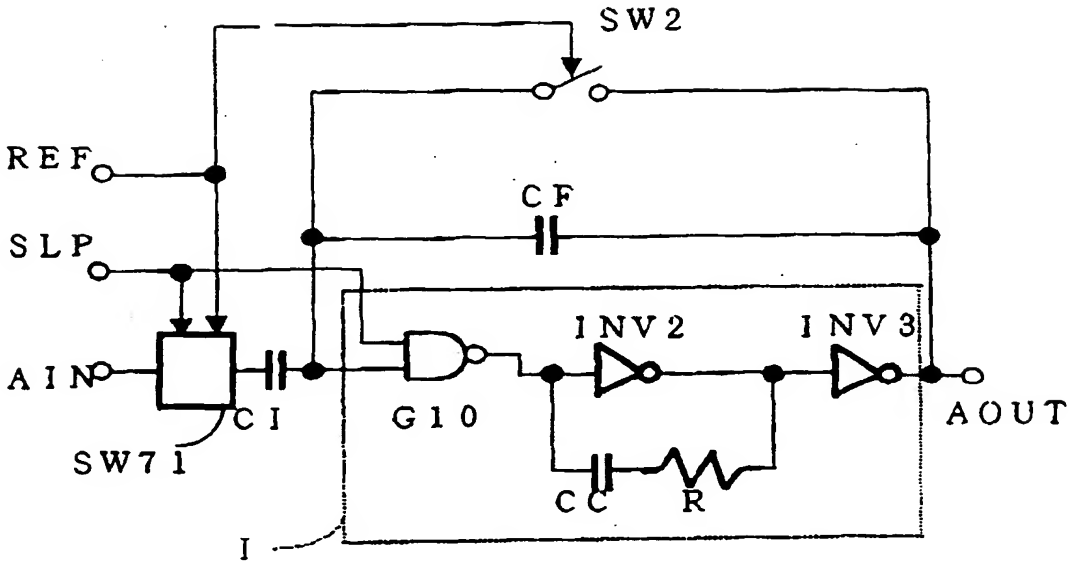


Fig.17

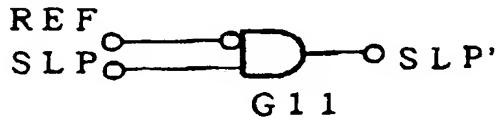
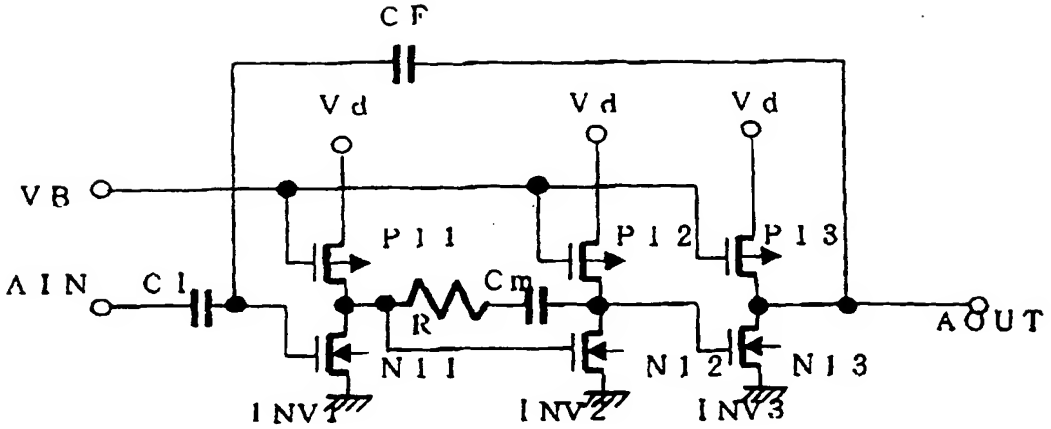


Fig.18

Fig.19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Vd
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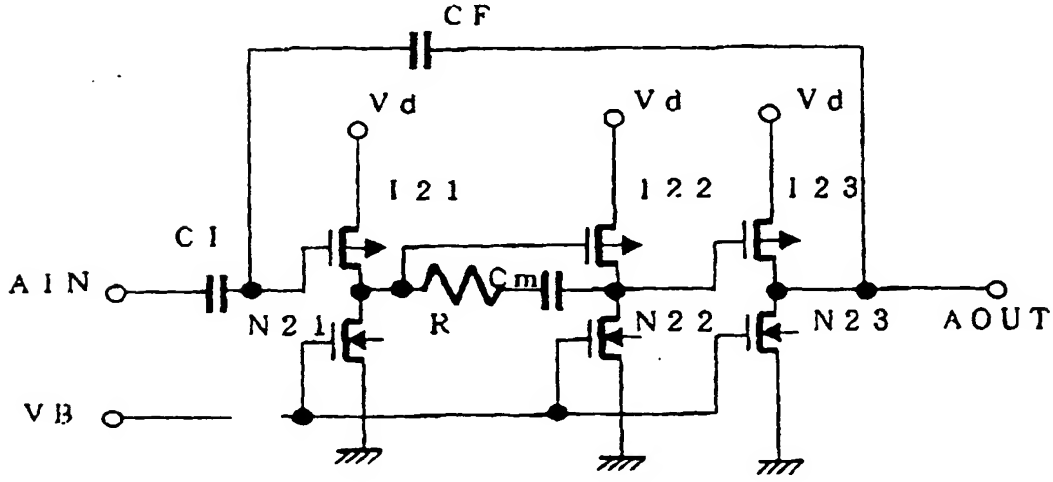
AIN
CI
Cm
R
AOUT
N11
N12
N13
INV1
INV2
INV3

Fig.20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Vd
Vd
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I22
I23
CI
AIN
Cm
N21
R
N22
N23
AOUT
VB

Fig.21

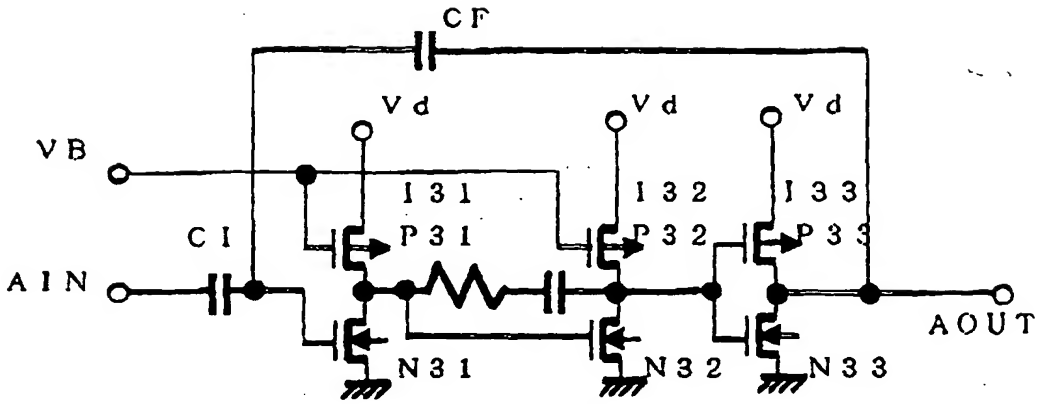
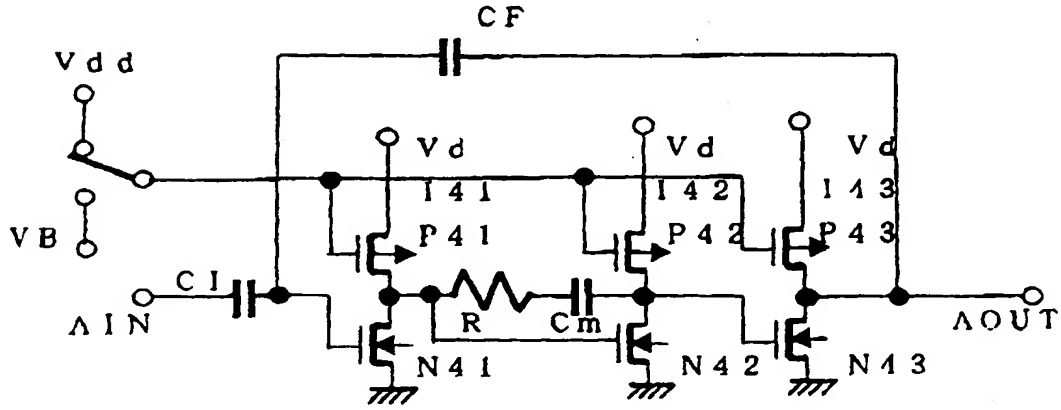
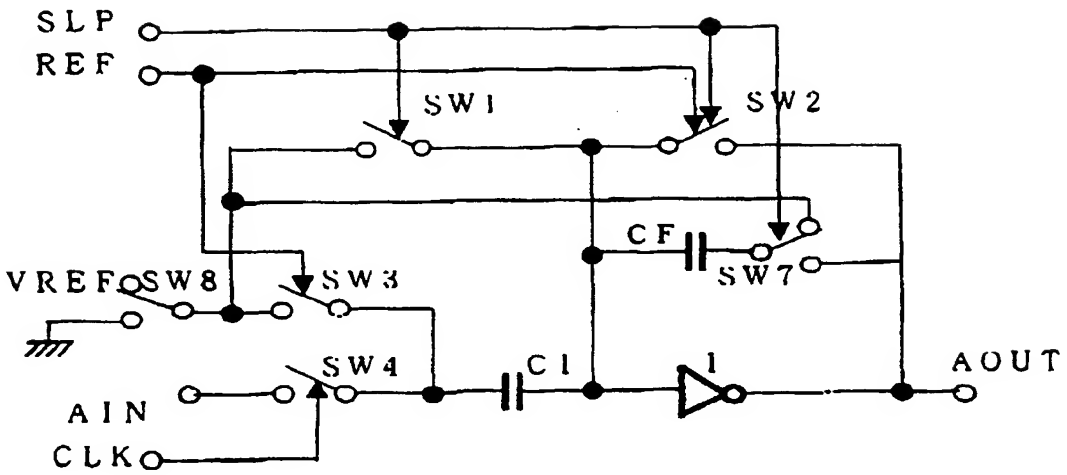


Fig.22



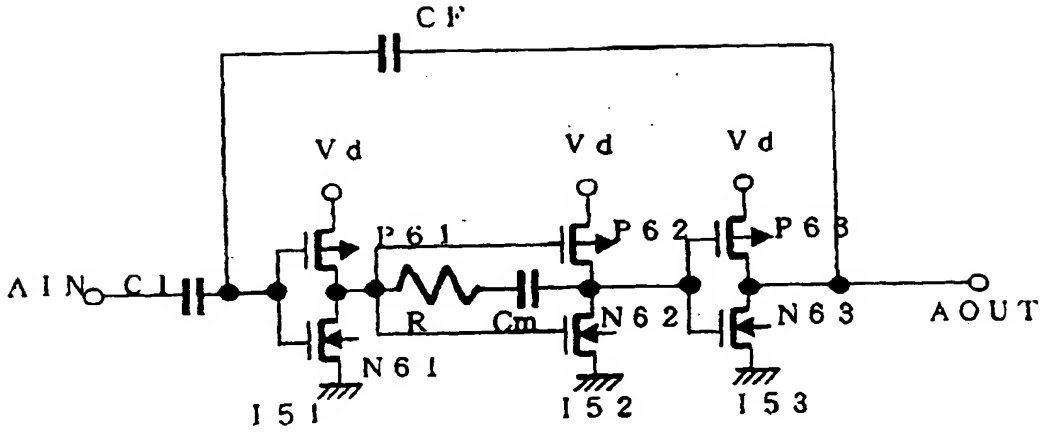
Prior Art

Fig.23



Prior Art

Fig.24



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EUROPEAN SEARCH REPORT

Application Number
EP 98 10 9867

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 5 142 238 A (WHITE BERT) 25 August 1992 * column 5, line 1 - column 10, line 57; figures 5,6,8 *	1-4,11, 12	H03F3/00 H03F1/30
A	EP 0 584 544 A (YOZAN INC) 2 March 1994 * column 2, line 4 - column 4, line 11; figures 1-6 *	1,2,9, 10,13, 15,16,21	
A	EP 0 110 130 A (NIPPON ELECTRIC CO) 13 June 1984 * the whole document *	1	
A	WO 92 09990 A (ITALTEL SPA) 11 June 1992 * abstract; figure 1A *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H03F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	20 August 1998	Tyberghien, G

CATEGORY OF CITED DOCUMENTS

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